

*Sub A<sup>1</sup>*  
 ✓ What is claimed is:

- 1 1. A field effect transistor comprising:
- 2 a substrate having a recess in a surface thereof, the recess having a
- 3 bottom portion and substantially vertical sidewalls;
- 4 a gate dielectric layer disposed superjacent the bottom portion of the
- 5 recess and adjacent the substantially vertical sidewalls;
- 6 a gate electrode overlying the gate dielectric layer; and
- 7 source/drain terminals disposed in the substrate in alignment with a pair of
- 8 laterally opposed gate electrode sidewalls;
- 9 wherein the source/drain terminals have an extension which extends
- 10 downwardly, from approximately the surface of the substrate, along the sidewalls
- 11 of the recess.

- Sub C<sup>2</sup>*  
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- 1 2. The transistor of Claim 1, further comprising a portion of the gate
  - 2 electrode that overlies an innermost portion of the source/drain extension:
  - 1 3. The structure of Claim 2, wherein the gate electrode conforms to the
  - 2 recessed channel.

- Sub A<sup>2</sup>*  
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- 1 4. A field effect transistor, comprising:
  - 2 a substrate having a recess in a surface thereof, the recess having bottom
  - 3 portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse
  - 4 angle with respect to the bottom portions of the recess;

5 a gate dielectric layer disposed superjacent the bottom portion of the  
 6 recess and adjacent the tapered sidewalls;  
 7 a gate electrode overlying the gate dielectric layer; and  
 8 source/drain terminals disposed in the substrate in alignment with a pair of  
 9 laterally opposed gate electrode sidewalls;  
 10 wherein the source/drain terminals have an extension which extends  
 11 downwardly, from approximately the surface of the substrate, along the sidewalls  
 12 of the recess.

*Sub C<sup>4</sup>*

1 5. The transistor of Claim 4, wherein a portion of the gate electrode that  
 2 overlies an innermost portion of the source/drain extension.

1 6. The transistor of Claim 4, wherein the gate electrode conforms to the  
 2 recessed channel.

*Sub A<sup>3</sup>*

1 7. A field effect transistor, comprising:  
 2 a substrate having a recess in a surface thereof, the recess having a  
 3 curvilinear shape;  
 4 a gate dielectric layer disposed superjacent the curvilinear recess;  
 5 a gate electrode overlying the gate dielectric layer; and  
 6 source/drain terminals disposed in the substrate in alignment with a pair of  
 7 laterally opposed gate electrode sidewalls;

8 wherein the source/drain terminals have an extension which extends  
 9 downwardly, from approximately the surface of the substrate, along the  
 10 curvilinear sides of the recess.

*Sub C6*

1 8. The transistor of Claim 6, wherein a portion of the gate electrode that  
 2 overlies an innermost portion of the source/drain extension.

1 9. The transistor of Claim 6, wherein the gate electrode conforms to the  
 2 recessed channel.

1 10. A method of making a microelectronic device, comprising:  
 2 forming a first layer over a substrate;  
 3 forming openings in the first layer, the openings exposing a portion of the  
 4 substrate, the openings having substantially vertical sidewalls;  
 5 forming a first spacer adjacent the sidewalls of the first layer openings;  
 6 forming a second spacer adjacent the first spacer;  
 7 etching a portion of the exposed substrate;  
 8 removing the second spacer;  
 9 forming a dielectric layer superjacent the exposed portions of the  
 10 substrate;  
 11 forming an electrode superjacent the dielectric layer; and  
 12 removing the first layer.

1 11. The method of Claim 10, wherein etching a portion of the exposed  
2 substrate comprises isotropically etching the substrate.

1 12. The method of Claim 10, wherein etching a portion of the exposed  
2 substrate comprises anisotropically etching the substrate.

1 13. The method of Claim 10, further comprising oxidizing the exposed  
2 portions of the substrate, and wherein the etching a portion of the exposed  
3 substrate comprises etching the oxidized portions of the substrate.

1 14. A method of forming a field effect transistor, comprising:  
2 depositing an etch stop layer and a damascene layer over a silicon  
3 substrate;  
4 removing portions of the damascene and etch stop layers to expose  
5 portions of the silicon, and form sidewalls in the damascene and etch stop  
6 layers;  
7 forming a first spacer layer along the sidewalls of the damascene layer  
8 and the etch stop layer;  
9 etching the exposed silicon;  
10 removing the second spacer; forming a gate dielectric layer superjacent  
11 the etched silicon; and depositing a gate electrode layer over the damascene  
12 and gate dielectric layers;  
13 planarizing the gate electrode layer so as to form a gate electrode;

- 14            removing the damascene, second spacer, and etch stop layers; and  
15            forming source/drain terminals self-aligned to the gate electrode.

1    15.    The method of Claim 14, wherein planarizing the gate electrode layer  
2    comprises chemical mechanical polishing using the damascene layer as a polish  
3    stop.

1    16.    The method of Claim 14, further comprising implanting ions into the silicon  
2    substrate.

1    17.    The method of Claim 14, further comprising implanting ions into the silicon  
2    substrate, after the first and second spacers are formed.

1    18.    The method of Claim 14, further comprising performing a channel implant  
2    into the silicon using the damascene, first spacer, and second spacer layers as  
3    implant masks.

1    19.    The method of Claim 14 wherein forming source/drain terminals  
2    comprises implanting ions of a first conductivity type into the silicon, adjacent to  
3    the gate electrode; forming third spacers adjacent to the gate electrode, and  
4    implanting ions of a first conductivity type into the silicon, adjacent to the third  
5    spacers.

1 20. The method of Claim 14, wherein etching the silicon comprises an  
2 anisotropic etch.

1 21. The method of Claim 14, wherein etching the silicon comprises an  
2 isotropic etch.

1 22. A method of forming a field effect transistor, comprising:  
2 depositing an etch stop layer and a damascene layer over a silicon  
3 substrate;  
4 removing portions of the damascene and etch stop layers to expose  
5 portions of the silicon, and form sidewalls in the damascene and etch stop  
6 layers;  
7 forming a first spacer layer along the sidewalls of the damascene layer  
8 and the etch stop layer, and a second spacer adjacent the first spacer layer;  
9 oxidizing the exposed silicon;  
10 etching the exposed oxidized silicon;  
11 removing the second spacer; forming a gate dielectric layer superjacent  
12 the etched silicon; and depositing a gate electrode layer over the damascene  
13 and gate dielectric layers;  
14 planarizing the gate electrode layer so as to form a gate electrode;  
15 removing the damascene, second spacer, and etch stop layers; and  
16 forming source/drain terminals self-aligned to the gate electrode.